IN THE CLAIMS:

On page 9, in line 1, cancel "Patent Claims" substitute --**I CLAIM AS MY INVENTION:**-- therefor.

Please cancel claims 1-6, substitute the following claims 7-12 therefor:

5   7.   A method for system simulation with simulated microcontrollers/microprocessors and appertaining peripheral modules, said method comprising the steps of:

in a first sequence of steps, simulating said

microcontroller/microprocessor and said peripheral modules with

10   predetermined signal patterns, said first sequence of steps having

markers inserted therein;

in a second sequence of steps, interrogating and evaluating states of said

system brought about by said simulation; and

interrupting said first sequence of steps for executing said second

15   sequence of steps as dictated by said markers inserted into said

first sequence, said second sequence of steps being executed in an

accelerated operational mode that is adapted to said evaluation.

8.   The method as claimed in claim 7, wherein said first sequence of steps provides a clock-cycle-based simulation of said

20   microcontroller/microprocessor and of said peripheral modules.

9.   The method as claimed in claim 7, wherein said first sequence of steps is a series of consecutive program codes.

10.   The method as claimed in claim 9, wherein said markers are formed by one of opcodes or opcode sequences that are not usually used in said

25   program code.

11.   The method as claimed in claim 7, wherein peripheral modules
that were specified during said second sequence of steps are functionally
cosimulated.

12.   A system for carrying out a method for system simulation with

5   simulated microcontrollers/microprocessors and appertaining peripheral
modules, said method comprising the steps of:

in a first sequence of steps, simulating said

microcontroller/microprocessor and said peripheral modules with

predetermined signal patterns, said first sequence of steps having

10   markers inserted therein;

in a second sequence of steps, interrogating and evaluating states of said

system brought about by said simulation; and

interrupting said first sequence of steps for executing said second

sequence of steps as dictated by said markers inserted into said

15   first sequence, said second sequence of steps being executed in an

accelerated operational mode that is adapted to said evaluation;

said system comprising:

a microprocessor control unit for simulating a module by generating

signal patterns with an essentially precise clock cycle and for

20   interrogating and evaluating states of said module that are

brought about by said simulation during a program interrupt by

activating an instruction set simulator.